

| Memory Type  | Maximum Size | On Chip? | Typical Use                |
|--------------|--------------|----------|----------------------------|
| GP Registers | 128 regs.    | yes      | Intermediate computation   |
| Inst. Cache  | 16 Kbytes    | yes      | Recently used instructions |
| Data Cache   | 8 Kbytes     | yes      | Recently used data         |
| Mini Cache   | 512 bytes    | yes      | Data that is reused once   |
| Write buffer | unspecified  | yes      | Write operation buffer     |
| Scratchpad   | 4 Kbytes     | yes      | IPC and synchronization    |
| Inst. Store  | 64 Kbytes    | yes      | Microengine instructions   |
| FlashROM     | 8 Mbytes     | no       | Bootstrap                  |
| SRAM         | 8 Mbytes     | no       | Tables or packet headers   |
| SDRAM        | 256 Mbytes   | no       | Packet storage             |

**Figure 18.8** Some of the elements in the memory hierarchy on Intel's IXP1200 available to the StrongARM processor. Larger memories are external to the chip.