

	clock	stage 1	stage 2	stage 3	stage 4	stage 5
Time ↓	1	inst. K	inst. K-1	inst. K-2	inst. K-3	inst. K-4
	2	inst. K+1	inst. K	inst. K-1	inst. K-2	inst. K-3
	3	inst. K+2	inst. K+1	inst. K	inst. K-1	inst. K-2
	4	inst. K+3	inst. K+2	inst. K+1	inst. K	inst. K-1
	5	inst. K+3	inst. K+2	inst. K+1	-	inst. K
	6	inst. K+3	inst. K+2	inst. K+1	-	-
	7	inst. K+4	inst. K+3	inst. K+2	inst. K+1	-
	8	inst. K+5	inst. K+4	inst. K+3	inst. K+2	inst. K+1

**Figure 20.4** An example pipeline in which instruction K+1 stalls at stage three to await the result from instruction K.