

	absolute addr.	used by	relative addr.
SDRAM read (32 regs.)	24 - 31	context 3 (8 regs.)	0 - 7
	16 - 23	context 2 (8 regs.)	0 - 7
	8 - 15	context 1 (8 regs.)	0 - 7
	0 - 7	context 0 (8 regs.)	0 - 7
SDRAM write (32 regs.)	24 - 31	context 3 (8 regs.)	0 - 7
	16 - 23	context 2 (8 regs.)	0 - 7
	8 - 15	context 1 (8 regs.)	0 - 7
	0 - 7	context 0 (8 regs.)	0 - 7
SRAM read (32 regs.)	24 - 31	context 3 (8 regs.)	0 - 7
	16 - 23	context 2 (8 regs.)	0 - 7
	8 - 15	context 1 (8 regs.)	0 - 7
	0 - 7	context 0 (8 regs.)	0 - 7
SRAM write (32 regs.)	24 - 31	context 3 (8 regs.)	0 - 7
	16 - 23	context 2 (8 regs.)	0 - 7
	8 - 15	context 1 (8 regs.)	0 - 7
	0 - 7	context 0 (8 regs.)	0 - 7

**Figure 20.8** Absolute and relative addresses used for the transfer registers on an Intel microengine. All external data transfers go through the transfer registers.