to onboard memory
to external memory
H0
H1
H2
H3
H4
S
D0
D1
D2
D3
D4
D5
D6
control memory arbiter
ingress queue
completion unit
egress queue
interrupts
exceptions
debug & inter.
hardware regs.
inter. bus control
embed. PowerPC
PCI bus
programmable protocol processors (16 picoengines)
ingress data store
ingress data iface
egress data iface
egress data store
instr. memory
classifier assist
bus arbiter
internal bus
ingress data store
frame dispatch
egress data store