Instruction	Description
Arithmetic, Rotate, And Shift Instructions	
ALU	Perform an arithmetic operation
ALU_SHF	Perform an arithmetic operation and shift
DBL_SHIFT	Concatenate and shift two longwords
Branch and Jump Instructions	
BR, BR=0, BR!=0, BR>0, BR>=0, BR<0, BR<=0, BR=count, BR!=count	Branch or branch conditional
BR_BSET, BR_BCLR	Branch if bit set or clear
BR=BYTE, BR!=BYTE	Branch if byte equal or not equal
BR=CTX, BR!=CTX	Branch on current context
BR_INP_STATE	Branch on event state
BR_!SIGNAL	Branch if signal deasserted
JUMP	Jump to label
RTN	Return from branch or jump
Reference Instructions	
CSR	CSR reference
FAST_WR	Write immediate data to thd_done CSRs
LOCAL_CSR_RD, LOCAL_CSR_WR	Read and write CSRs
R_FIFO_RD	Read the receive FIFO
PCI_DMA	Issue a request on the PCI bus
SCRATCH	Scratchpad memory request
SDRAM	SDRAM reference
SRAM	SRAM reference
T_FIFO_WR	Write to transmit FIFO
Local Register Instructions	
FIND_BST, FIND_BSET_WITH_MASK	Find first 1 bit in a value
IMMED	Load immediate value and sign extend
IMMED_B0, IMMED_B1, IMMED_B2, IMMED_B3	Load immediate byte to a field
IMMED_W0, IMMED_W1	Load immediate word to a field
LD_FIELD, LD_FIELD_W_CLR	Load byte(s) into specified field(s)
LOAD_ADDR	Load instruction address
LOAD_BSET_RESULT1, LOAD_BSET_RESULT2	Load the result of find_bset
Miscellaneous Instructions	
CTX_ARB	Perform context swap and wake on event
NOP	Skip to next instruction
HASH1_48, HASH2_48, HASH3_48	Perform 48-bit hash function 1, 2, or 3
HASH1_64, HASH2_64, HASH3_64	Perform 64-bit hash function 1, 2, or 3

Figure 20.1 The instruction set of a microengine on the Intel IXP1200.