

	clock	stage 1	stage 2	stage 3	stage 4	stage 5
Time ↓	1	inst. 1	-	-	-	-
	2	inst. 2	inst. 1	-	-	-
	3	inst. 3	inst. 2	inst. 1	-	-
	4	inst. 4	inst. 3	inst. 2	inst. 1	-
	5	inst. 5	inst. 4	inst. 3	inst. 2	inst. 1
	6	inst. 6	inst. 5	inst. 4	inst. 3	inst. 2
	7	inst. 7	inst. 6	inst. 5	inst. 4	inst. 3
	8	inst. 8	inst. 7	inst. 6	inst. 5	inst. 4

Figure 20.2 Illustration of a five-stage execution pipeline used by a microengine on the IXP1200. Once the pipeline is full, the microengine completes one instruction on each clock cycle.